Hall Ticket Number:

Code No. : 13646 S

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (I.T) III-Semester Supplementary Examinations, August-2022

Digital Electronics and Logic Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Convert decimal +49 and -49 to binary, using the signed-2's-complement representation, with enough digits to accommodate the numbers.	2	1	1	1
2.	Reduce the following Boolean expressions to the indicated number of literals: **A'C '+ ABC + AC'** ------- to three literals	2	1	1	1
3.	Give a truth table for BCD to Excess-3 code converter.	2	1	2	1
4.	Draw 4-Bit adder circuit.	2	1	2	1
5.	Give the definition of synchronous and asynchronous inputs of flipflops and mention the disadvantage of JK flipflop and suggest the methods to overcome.	2	1	3	1
6.	Explain how a flip flop can be used as divide by 2 counter.	2	1	3	1
7.	Reduce the number of states in the following state table and tabulate the reduced state table.	2	2	4	1
8.	A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are $J_A = Bx + B'y'$ $K_A = B'xy'$ $J_B = A'x$ $K_B = A + xy'$ $z = Ax'y' + Bx'y'$ Draw the logic diagram.	2	1	4	1
9.	Explain how the ASM chart differs from a conventional flow chart.	2	1	4	1

Present State	Next State $x=0$	Next State $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

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10.	Write the differences between synchronous and asynchronous sequential circuit.	2	2	4	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Find all the prime implicants for the following Boolean functions, and determine which are essential: **F (A, B, C, D) =∑ (2,3,4,5,6,7,9,11,12,13)**	4	2	1	2
b)	Simplify the following functions, and implement them with two-level NAND gate circuits: **F (A, B, C, D) = AC' D' + A 'C + ABC + AB 'C + A' C' D'**	4	2	1	2
12. a)	Implement Full adder with 3*8 decoder and write a VHDL code for implementing Full adder.	4	2	2	1
b)	Simplify the following Boolean functions, implement with a PAL: W (A, B, C, D) = ∑2, 12, 13) X (A, B, C, D) = ∑ (7, 8, 9, 10, 11, 12, 13, 14, 15) Y (A, B, C, D) = ∑ (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15) Z (A, B, C, D) = ∑(1, 2, 8, 12, 13) and write suitable PAL programming table.	4	3	2	2
13. a)	Design 3 -Bit Synchronous Up/Down Counter and Write a VHDL code for JK Flip-Flop.	5	3	4,5	2
b)	Design a modulo-6 counter using a T flip flop.	3	3	4	2
14. a)	Distinguish between Mealy and Moore State machines.	4	3	4	2
b)	Design a sequence detector in a Mealy model, which detects the sequence 1001 from the continue binary sequences at its input x, construct a circuit in such a way that, it should generate 1 at its output Z, when 1001 sequence detected otherwise 0. (One-bit overlapping case also can be considered).	4	4	4	2
15. a)	Explain the different types of hazards in digital circuits.	4	2	4	2
b)	Explain the different components used in ASM charts.	4	2	4	1
16. a)	Explain about different tasks and CAD tools in designing digital circuits.	4	2	5	1
b)	Implement 8*1 Mux with 2*1 Multiplexers.	4	3	2	2
17.	Answer any ***two*** of the following:				
a)	Draw the block diagram of Bidirectional shift Register with parallel load and explain its operation with suitable functional diagram.	4	3	3	1
b)	Design Mod-6 asynchronous counter, give relevant state table.	4	3	4	2
c)	Explain the steps in digital hardware design flow.	4	2	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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